UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Heinen	Group Art Unit:	2857
Application No.:	10/557,104	Examiner:	Charioui, M.
Filed:	27 November 2006	Confirmation No.:	5365
Subject:	INTEGRATED CIRCUIT WITH BIT ERROR TEST CAPABILITY		
Atty Docket No.:	20031035-02		

AMENDMENT UNDER 37 CFR 1.111

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Claims 1-13 were presented for examination. In a non-final Office Action mailed October 3, 2008, all claims were rejected.

In response to the Office Action, Applicants hereby request reconsideration as follows:

A **Claims** listing begins on page 2.

Amendment to the **specification** to add paragraphs begins on page 6.

Remarks begin on page 7.